Remarks

I. Status of claims

Claims 1, 3-11, and 23-27 now are pending.

Claims 2 and 12-22 have been canceled.

Claims 23-27 have been added.

II. Claim rejections under 35 U.S.C. § 102

The Examiner has rejected claim 1 under 35 U.S.C. § 102(e) over Moriizumi (U.S. 6,485,814). Moriizumi, however, does not teach or suggest anything about forming a via that extends through a wafer from a contact of a microelectronic device, which is on a front side of the wafer, to the back side of the wafer, as now recited in claim 1.

Moriizumi discloses a method of forming a circuit board that consists of a multi-layered thin film circuit 1 and an underlying substrate 6. A solder bump 4 electrically connects a contact pad of an LSI chip the front side of the multi-layered thin film circuit 1. The multi-layered thin film circuit 1 electrically connects the solder bump 4 to a conductor 8 on the back side of the multi-layered thin film circuit 1. The substrate 6 includes a hole 10 for receiving a solder bump 12 that provides a strong and reliable means for attaching an I/O pin 5 of the circuit board to the conductor 8 on the back side of the multi-layered thin film circuit 1.

Thus, in Moriizumi's approach, the LSI chips are mounted to the multi-layered thin film circuit 1, they are not on the front side of the substrate 6. Consequently, the hole 10 in Moriizumi's substrate 6 does not extend through the substrate 6 from a contact of an LSI chip, which is on a front side of the substrate 6, to the back side of the substrate 6.

For at least these reasons, the Examiner's rejection of claim 1 under 35 U.S.C. § 102(e) over Moriizumi now should be withdrawn.

Claim 1 also has been amended to incorporate the feature of claim 2 that the width of the via is at most 80 μm. The Examiner rejected claim 2 under 35 U.S.C. § 103(a) over Moriizumi in view of Thomas (U.S. 6,326,689).

Thomas discloses a method of forming a contact on a back side of a die that is electrically connected to a contact of an active region by a backside contact interconnect that

extends over sloped sidewalls formed at the edge of the die. The sloped sidewalls are formed by etching a hole from the back side of a substrate and across the logical boundary between two dice sharing the same opening (see col. 5, lines 48-51). The backside contact interconnect is formed on two sidewalls of the opening. The two dice are separated such that a portion of the active region contact and a respective backside contact interconnect remains with each die (see col. 6, lines 6-9). According to Thomas,

> The width of the active region contact 310 at the bottom of the opening in a direction across the logical boundary is at least the kerf dimension of the device to be employed to separate the two die (e.g., saw or scribe), plus the required width of the contact area needed for conductive lines formed on the sidewalls of opening 304 to connect active region contact 310 to contact pads on the backside surface of the substrate. In the exemplary embodiment, active region contact is at least 250 μm in width. Opening 304 in the exemplary embodiment is 1250 μm wide at the backside surface of substrate 302, 250 μm wide at the bottom, and 350 μm deep.

With respect to the features of claim 2, the Examiner has asserted that:

> In re claims 2-3, Moriizumi et al. do not expressly teach that the sloped via is no wider than 80 μm or 50 μm.
>
> Thomas, however, in analogous art of forming sloped via contact, teach that the width of the sloped via involves the required dimension of the contact area needed for conductive material formed in the sidewalls of the sloped via (col. 5, lines 52-63).
>
> Therefore, one of ordinary skill in the art, at the time the invention was made, would have been motivated to optimize the width of the sloped via, as suggested by Thomas, in the method of Moriizumi et al. for the purpose of obtaining a suitable dimension of contact area associated with the sloped via.

The Examiner's assertion regarding Thomas' teaching is incorrect. As explained above, Thomas teaches that the width of the bottom of the opening at the active region contact is at least the kerf dimension of the die separation tool. According to Thomas, this dimension is at least 250 μm (see col. 5, lines 59-63). Since the hole opening increases from the active region contact to the back side of the substrate, the width of the hole opening is

smallest at the active region contact and is largest at the backside of the substrate. Thomas does not even hint that the width of the hole could be at most 80 μm.

Since neither Moriizumi nor Thomas teaches or suggests anything about forming a via with a width of at most 80 μm, no possible combination of these references would have led one of ordinary skill in the art to such a via. As a result, the Examiner's rationale in support of his obviousness rejection amounts to no more than the impermissible "obvious to try" rationale, which is not the proper standard under 35 U.S.C. § 103 (see MPEP § 2145.X.B).

Moreover, the object of Moriizumi's invention is to provide a hole 10 in a substrate 6 for receiving a solder bump 12 that provides a strong and reliable means for attaching an I/O pin 5 of the circuit board. In Thomas' approach, the holes are cut along the logical boundaries between adjacent dice. When the dice are separated from one another, the holes are converted to notches at the edges of the dice. These notches, however, are not suitable for receiving a solder bump that provides a strong and reliable means for attaching an I/O pin to a die. Accordingly, one of ordinary skill in the art at the time the invention was made would not have looked to the teaching of Thomas for guidance as to how the teachings of Moriizumi relating to the I/O pin attachment holes might be modified.

For at least the reasons explained above, claim 1 is patentable over any permissible combination of Moriizumi and Thomas.

III. Claim rejections under 35 U.S.C. § 103

A. Claims 3-7

The Examiner has rejected claims 2-7 under 35 U.S.C. § 103(a) over Moriizumi in view of Thomas (U.S. 6,326,689). The features of claim 2 have been incorporated into claim 1 and claim 2 has been canceled.

Each of claims 3-7 incorporates the features of independent claim 1 and therefore is patentable over Moriizumi and Thomas for at least the same reasons explained above.

B. Claim 8

The Examiner has rejected claim 8 under 35 U.S.C. § 103(a) over Moriizumi in view of Thomas and Wang (U.S. 6,662,419).

Claim 8 incorporates the features of independent claim 1. Wang does not make-up for the failure of Moriizumi and Thomas to teach or suggest the features of claim 1 discussed above. Therefore, claim 8 is patentable over Moriizumi, Thomas, and Wang for at least the same reasons explained above in connection with claim 1.

C. Claims 9 and 10

The Examiner has rejected claims 9 and 10 over Moriizumi, Thomas, Wang and Hubacher (U.S. 5, 536,677).

Each of claims 9 and 10 incorporates the features of independent claim 1. Hubacher does not make-up for the failure of Moriizumi, Thomas, and Wang to teach or suggest the features of claim 1 discussed above. Therefore, claims 9 and 10 are patentable over Moriizumi, Thomas, Wang, and Hubacher for at least the same reasons explained above in connection with claim 1.

D. Claim 11

The Examiner has rejected claim 11 over Moriizumi, Thomas, and Siniaguine (U.S. 6,184,060).

Claim 11 incorporates the features of independent claim 1. Siniaguine does not make-up for the failure of Moriizumi and Thomas to teach or suggest the features of claim 1 discussed above. Therefore, claim 11 is patentable over Moriizumi, Thomas, and Siniaguine for at least the same reasons explained above in connection with claim 1.

IV. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-1078.

Respectfully submitted,

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